A Fast Frequency-Switching Synthesizer with an Integration Circuit

Hideyuki Nosaka, *Member, IEEE,* Tadao Nakagawa, *Member, IEEE,* and Akihiro Yamagishi

***Abstract*— A new type of direct frequency synthesizer, which can complete frequency switching in less than a microsecond, is proposed. This yields low-spurious outputs by using a low-power analog integration circuit, whose operating principle is similar to a digital accumulator. Experimental results demonstrate successful frequency synthesizer operation.**

***Index Terms*— Delta–sigma modulation, frequency synthesizers, jitter elimination, low-power consumption, spread-spectrum communication.**

I. Introduction

FAST frequency switching of frequency synthesizers has become an important requirement in advanced wireless communication systems. Fast frequency switching inside the guard time enables dynamic channel assignment in time-division multiple-access (TDMA) systems. Fast frequency switching also enables the frequency-hopping spread-spectrum (FH-SS) technique, which has better performance than the direct-sequence spread-spectrum (DS-SS) technique with respect to near–far effect [1]. Direct digital synthesizers (DDS's) are able to provide the required fast frequency switching because they have no feedback loop, such as that used in phase-locked-loop (PLL) frequency synthesizers. DDS's have certain disadvantages, however, such as narrow tuning bandwidths and large power consumption. The most popular DDS is the sine output DDS [2], the tuning bandwidth of which is limited by the read only memory (ROM) access time. Since the use of larger ROM increases both ROM access time and power consumption, efforts have been made to reduce ROM size without degrading the spurious performance [3], [4]. We have proposed two types of ROM-less DDS's, i.e., a DDS with an interpolation circuit [5] and a DDS with a digitally controlled delay generator [6], in an attempt to achieve a high-speed low-power frequency synthesizer. Recently, an alternative ROM-less DDS, whose maximum output frequency is not limited to half the clock frequency, has been proposed [7]. These ROM-less DDS's have the potential for realizing a high-speed low-power frequency synthesizer; however, a high-speed digital circuit, which includes an accumulator, consumes a lot of power.

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H. Nosaka is with NTT Wireless Systems Laboratories, Yokosuka-shi 239-0847, Japan.

T. Nakagawa is with STE Telecommunication Engineering Company, Ltd., Tokyo 100-0011, Japan.

A. Yamagishi is with NTT System Electronics Laboratories, Atsugi-shi 243-0122, Japan.

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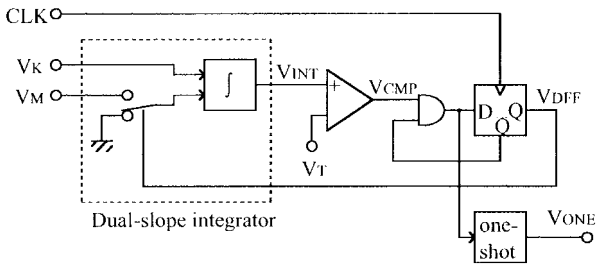


Fig. 1. Configuration of the jitter-free V/F.

This paper presents a new concept for direct frequency synthesis, which uses an analog integrator to create the same waveforms that the digital accumulator creates with an interpolation circuit. This synthesizer outputs square waves with low spurious components. A digital resetting circuit is adopted to restrain frequency drift in the output signal. Experimental results confirm the validity of the concept.

II. Principle

The operation of the proposed frequency synthesizer can be characterized as a two-step development from a conventional dual-slope integrating voltage-to-frequency (V/F) converter [8]. The first step is a jitter-reduction method which offers a jitter-free V/F, and the second step is a periodical resetting method, which restrains frequency drift in the output signal. We propose two types of integrators for the frequency synthesizer. One has static digital-to-analog converters (D/A's), and the other has a dynamic D/A.

A. Jitter-Free V/F

Proposed jitter-free V/F contains a dual-slope integrator, comparator, and some control logic, as shown in Fig. 1. The dual-slope integrator consists of a voltage switch and a differential integrator. V_K and V_M are input voltages which satisfy the relation

$$0 < 2V_K \leqq V_M. \tag{1}$$

The waveforms of the jitter-free V/F for $V_K = 3$ and $V_M = 8$ are shown in Fig. 2(a). Waveforms are clock (CLK), the integrator output $(V_{\rm INT})$, the comparator output $(V_{\rm CMP})$, delay flip–flop (D-FF) output $(V_{\rm DFF})$, and the one-shot multivibrator output $(V_{\rm ONE})$. The voltage switch selects the ground level if the initial integrator output $V_{\rm INT}$ is smaller than the threshold voltage V_T. Then $V_{\rm INT}$ increases with a slope of $V_K = 3$. We call this interval the increasing period. When

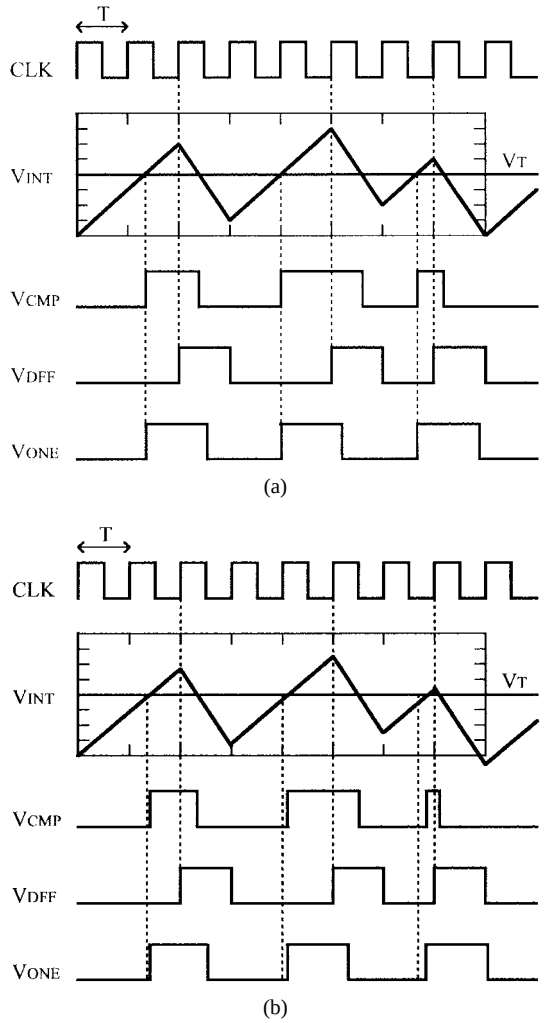


Fig. 2. Waveforms of the jitter-free V/F for (a) $V_K = 3$ and $V_M = 8$ and (b) $V_K = 2.9$ and $V_M = 8$.

$V_{\rm INT}$ reaches V_T, the comparator output switches to high level. The D-FF, however, keeps its previous output and the voltage switch remains at the ground level. The next clock pulse causes the D-FF to switch to high level. This causes the voltage switch to select the input voltage V_M, after which, $V_{\rm INT}$ decreases with a slope of $V_K - V_M = -5$. We call this interval the decreasing period. Since the magnitude of the slope $|V_K - V_M|$ is larger than that of the increasing period $|V_K|$, the integrator output $V_{\rm INT}$ is decreased below V_T within one clock cycle. Thus, any decreasing period continues for just one clock cycle regardless of input voltages.

When both V_K and V_M are integers, the integrator operates periodically with a period of $V_M \cdot T$, where T is clock cycle. The operation period $V_M \cdot T$ contains $(V_M - V_K) \cdot T$ increasing periods and $V_K \cdot T$ decreasing periods. In Fig. 2(a), the overall increasing period is $5 \cdot T$ and the overall decreasing period is $3 \cdot T$ during an operation period of $8 \cdot T$. Since each decreasing period is one clock cycle, the time intervals of rising edges of $V_{\rm CMP}$ pulses stay constant. The one-shot output $V_{\rm ONE}$ has no spurious components because both the pulse widths and time intervals of the rising edges are constant. The fundamental

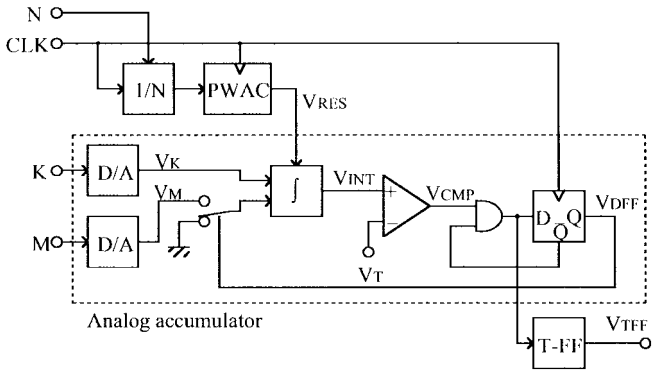


Fig. 3. Configuration of the frequency synthesizer with static D/A's.

frequency is given by

$$f_{\rm ONE} = \frac{V_K}{V_M} f_{\rm CLK} \tag{2}$$

where $f_{\rm CLK}$ is the clock frequency. On the other hand, $V_{\rm DFF}$, which corresponds to the conventional dual-slope integrating V/F output, also contains V_K pulses during $V_M \cdot T$, thus, the average frequency of $V_{\rm DFF}$ is expressed by (2). However, the momentary frequency varies periodically. Thus, $V_{\rm DFF}$ contains large spurious components.

The waveforms of the jitter-free V/F for $V_K = 2.9$ and $V_M = 8$ is shown in Fig. 2(b). In this case, each decreasing period is also one clock cycle, thus the intervals of rising edges of $V_{\rm CMP}$ pulses are constant. In particular, $V_{\rm ONE}$ has no spurious components for continuous variation of input voltages. The fundamental frequency is also given by (2) in the case of noninteger V_K or V_M. The one-shot can be replaced by a toggle flip–flop (T-FF) that operates at the rising edge of the input signal. In this case, the fundamental frequency of the synthesizer output is given by a half times equation (2).

B. Frequency Synthesizer with Static D/A's

The jitter-free V/F produces low spurious signals. However, it is difficult to apply this V/F as a local oscillator because of difficulty in obtaining frequency accuracy. For example, a little divergence in V_K or V_M causes significant divergence in the output frequency. In the proposed frequency synthesizer, a periodical resetting method is adopted in order to restrain unexpected frequency drift.

The configuration of proposed frequency synthesizer with static D/A's is shown in Fig. 3. The frequency synthesizer consists of a pair of D/A's, voltage switch, integrator, voltage comparator, AND gate, D-FF, frequency divider, pulsewidth adjusting circuit (PWAC), and T-FF. The division ratio of the frequency divider N can be chosen from the relation

$$N = L \frac{M}{G} \tag{3}$$

where G is the greatest common divisor (g.c.d.) between K and M, and L is an integer greater than or equal to one.

The waveforms of the frequency synthesizer are shown in Fig. 4 for $M = 8$, $K = 3$, and $N = 8$. The PWAC output $V_{\rm RES}$, contains one pulse within a period of $N \cdot T$. The PWAC adjusts the pulsewidth of $V_{\rm RES}$ to be T. In turn,

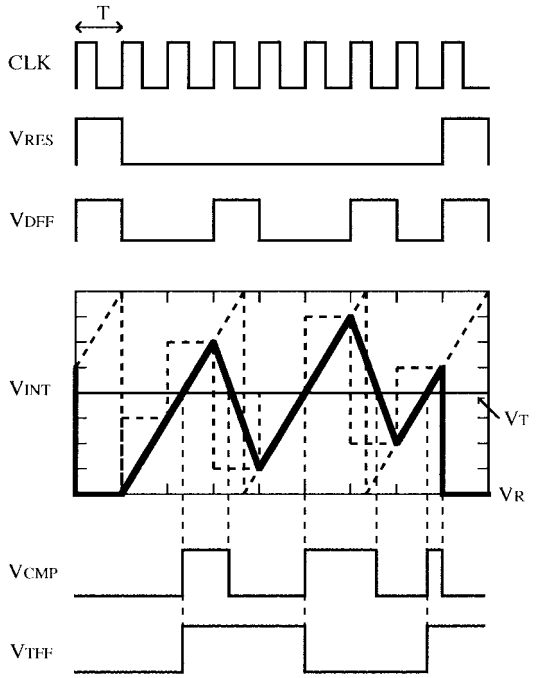


Fig. 4. Waveforms of the frequency synthesizer with static D/A's.

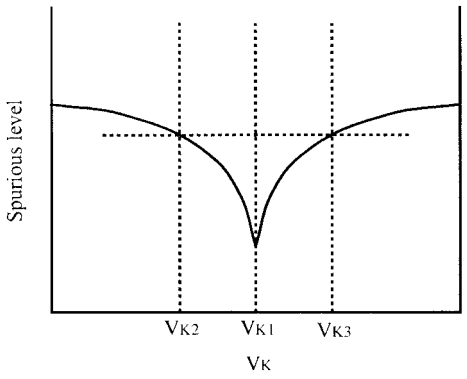


Fig. 5. Schematic relation between V_K and spurious level.

V_{RES} acts as the resetting signal for the integrator output V_{INT}. Therefore, if voltage drift occurs in V_{INT} for any reason, V_{INT} is periodically modified at the beginning of every period of $N \cdot T$. This resetting method restrains the frequency drift in the synthesizer output. The synthesizer output V_{TFF} becomes a square waveform with duty cycle of exactly 50%. The fundamental frequency is given by

$$f_{\mathrm{TFF}} = \frac{1}{2}\frac{K}{M} f_{\mathrm{CLK}}. \tag{4}$$

The T-FF can be replaced by a one-shot that operates at the rising edge of the input signal. In this case, the fundamental frequency of the synthesizer output is given twice by (4).

The momentary frequency drift, which can occur within a period of $N \cdot T$, causes a certain amount of spurious components. A schematic relation between V_K and spurious level is shown in Fig. 5. The minimum spurious level is observed when V_K is the analytical voltage V_{K1}. The permissible accuracy of V_K can be estimated experimentally if the highest permissible level of spurious components is known. For example, assuming that permissible level of spurious components is the horizontal dotted line in Fig. 5, the permissible accuracy of V_K can be estimated as $(V_{K3} - V_{K2})/V_{K1}$.

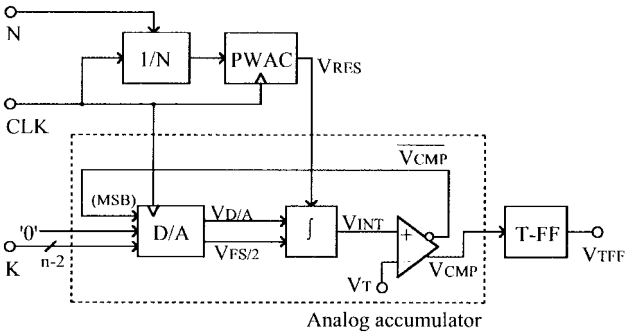


Fig. 6. Configuration of the frequency synthesizer with a dynamic D/A.

The power consumption of the frequency synthesizer that uses static D/A's is expected to be reduced dramatically when compared with that of DDS's, including ROM-less DDS's. Narrow-bandwidth D/A's can be used as the static D/A's. The voltage switch, however, restrains the highest clock frequency. A frequency synthesizer with a dynamic D/A (see Section II-C) is a solution which solves this problem by using a high-speed D/A.

C. Frequency Synthesizer with a Dynamic D/A

The configuration of the proposed frequency synthesizer that uses a dynamic D/A is shown in Fig. 6. The frequency synthesizer consists of an n-bit D/A, integrator, voltage comparator, frequency divider, PWAC, and T-FF. Division ratio of the frequency divider N can be chosen from (3), where M is given by 2^{n-1}, and n is the resolution of the D/A.

The waveforms of the frequency synthesizer are shown in Fig. 7 for $n = 4$ (namely $M = 8$), $K = 3$ and $N = 8$. The PWAC output V_{RES} contains one pulse within a period of $N \cdot T$. The D/A output $V_{\mathrm{D/A}}$ varies its voltage between two levels $V_{\mathrm{D/A}}(K)$ and $V_{\mathrm{D/A}}(K+M)$, which are proportional to K and $K+M$, respectively. Fig. 8 shows the relation of $V_{\mathrm{D/A}}$ and $V_{FS/2}$, where $V_{FS/2}$ is a constant voltage proportional to M (the median voltage in the D/A). The integrator integrates the differential voltage, $V_{\mathrm{D/A}} - V_{FS/2}$. V_{RES} resets the integrator periodically. This initialization reforms V_{INT}, which is assumed to drift easily. The time of coincidence of V_{INT} and the threshold voltage V_T is detected by the voltage comparator as rising edges of the pulses from the voltage comparator, V_{CMP}. The intervals of rising edges of V_{CMP} pulses are constant because the period when V_{INT} decreases is one clock cycle for $K \leq 2^{n-2}$. The T-FF output V_{TFF} becomes a square waveform with duty cycle of exactly 50% when the T-FF operates at the rising edge of the input signal. The fundamental frequency is given by (4). The T-FF can be replaced by a one-shot. In this case, the fundamental frequency of the synthesizer output is given twice by (4).

The power consumption of the frequency synthesizer that uses a dynamic D/A is expected to be reduced when compared with that of DDS's, including ROM-less DDS's. The circuit scale of the analog part and the D/A is similar to the ROM-

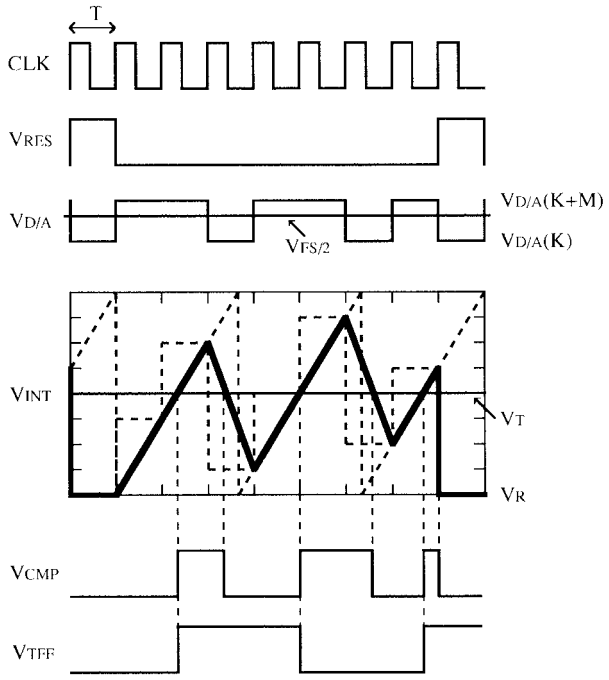


Fig. 7. Waveforms of the frequency synthesizer with a dynamic D/A.

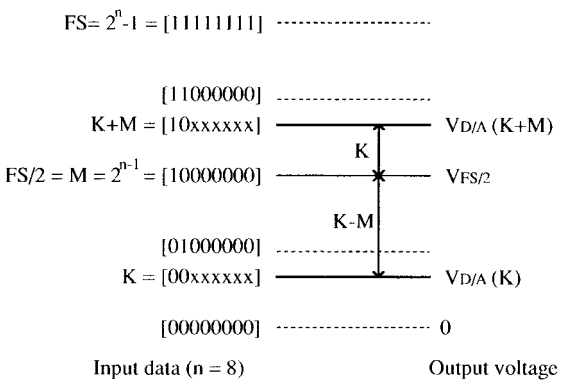


Fig. 8. Output voltages of the D/A.

less DDS [5], however, the gate count of the digital part, which dominates the power consumption in the synthesizer, is considerably reduced in comparison with that of the DDS's. An m-bit accumulator, which is used in DDS's, consists of an m-bit full adder and an m-bit latch, and all gates operate at the clock frequency. On the other hand, a binary counter, which is used in this frequency synthesizer, consists of several T-FF's, but only one T-FF operates at the clock frequency and the other T-FF's operate at lower frequencies. This means that at a given clock frequency, this frequency synthesizer can operate at a much lower power level than a DDS.

III. Experimental Results

A. Jitter-Free V/F

To confirm the operation principle, the proposed V/F and frequency synthesizers were constructed by combining discrete components. The V/F, shown in Fig. 1, was constructed by complementary metal–oxide–semiconductor (CMOS) standard logic. Fig. 9 shows measured waveforms as observed on an oscilloscope. The clock frequency f_{CLK} was 1 MHz and the input voltages V_M and V_K was 4 and 1.5 V, respectively. Measured waveforms were the clock (CLK), integrator output (V_{INT}), D-FF output (V_{DFF}), and one-shot output (V_{ONE}). The fundamental frequency of the one-shot was expected to be 375 kHz.

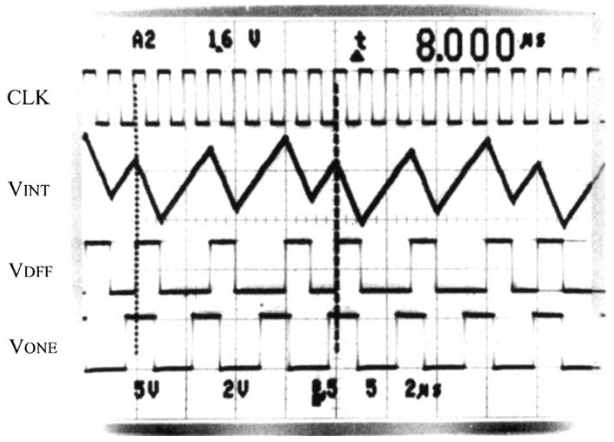


Fig. 9. Measured waveforms of the jitter-free V/F.

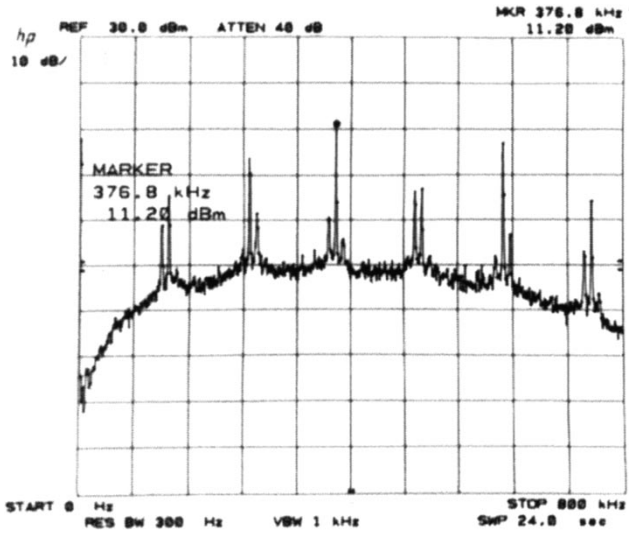
Fig. 10(a) shows measured spectra of the D-FF output and (b) shows the T-FF output when the one-shot in Fig. 1 was replaced by a T-FF. The D-FF output, which corresponds to conventional dual-slope integrating V/F output, contained fundamental frequency $f_{\mathrm{DFF}} = 375$ kHz. This signal, however, also contained high-level spurious components. The highest spurious level was -6 dBc. On the other hand, the T-FF output, which corresponds to proposed jitter-free V/F output, had a fundamental frequency $f_{\mathrm{TFF}} = 187.5$ kHz. Spurious components were significantly reduced in comparison with the D-FF output. The highest spurious level was -44 dBc. The output frequency varied continuously as V_K changed.

B. Frequency Synthesizer with Static D/A's

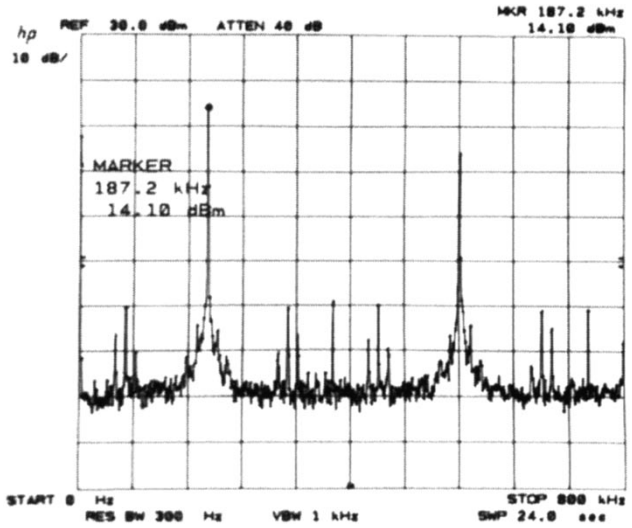
The frequency synthesizer, shown in Fig. 3, was constructed by emitter coupled logic (ECL). In this experiment, V_M and V_K were directly given by programmable power sources in place of D/A's. Fig. 11 shows measured waveforms as observed on an oscilloscope for $f_{\mathrm{CLK}} = 10$ MHz, $V_M = 1.6$ V, $V_K = 0.6$ V, and $N = 8$. The input voltages corresponded to $M = 8$ and $K = 3$. Measured waveforms were the clock (CLK), PWAC output (V_{RES}), D-FF output (V_{DFF}), integrator output (V_{INT}), comparator output (V_{CMP}), and T-FF output (V_{TFF}).

Fig. 12 shows the spectrum of V_{TFF}, given the same condition as Fig. 11. The T-FF output had a fundamental frequency $f_{\mathrm{TFF}} = 1.875$ MHz. The highest spurious level was -50 dBc.

Fig. 13 shows the relation between V_K and spurious level for $f_{\mathrm{CLK}} = 1$ MHz, $V_M = 2.0$ V, $V_K \approx 0.75$ V, and $N = 8$. The fundamental frequency $f_{\mathrm{TFF}} = 187.5$ kHz was observed in the voltage range $0.7\ \mathrm{V} < V_K < 0.774$ V. This fundamental frequency corresponded to $M = 8$, $K = 3$. The minimum spurious level -59 dBc was observed at the analytical value

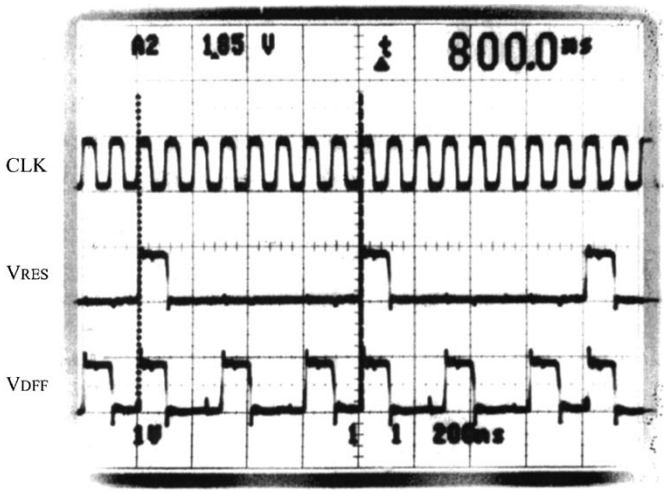


(a)

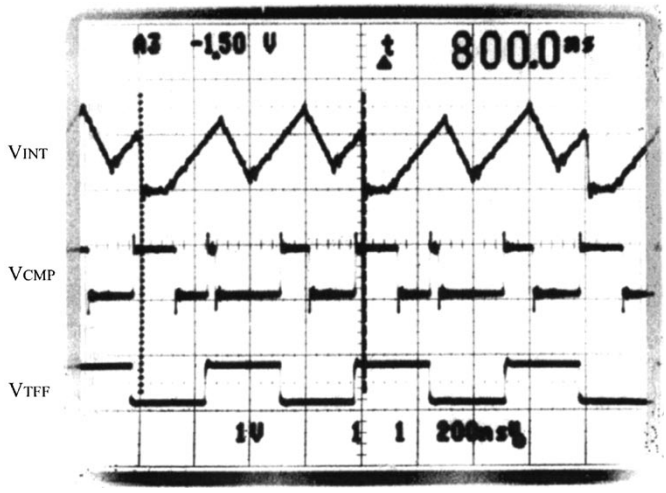


(b)

Fig. 10. Spectra of (a) the D-FF output, V_{DFF} and (b) the V/F output, V_{TFF}. H: DC-800 kHz, V: 10 dB/div.



(a)



(b)

Fig. 11. Measured waveforms of the frequency synthesizer with static D/A's.

$V_K = 0.75$ V. Fig. 13 shows that the permissible accuracy of V_K was roughly 1.2% when the permissible level of spurious components was -40 dBc.

C. Frequency Synthesizer with a Dynamic D/A

The synthesizer shown in Fig. 6 was created by combining discrete components. In this experiment, an 8-b D/A ($n = 8$) and a 4-b binary counter were employed. Here, $V_{FS/2}$ was supplied by a programmable power source. Fig. 14 shows waveforms of the synthesizer measured on an oscilloscope. The signal symbols on the left side of the figure correspond to those in Fig. 7. Note that the polarity of $V_{\mathrm{D/A}}$ is different from that in Fig. 7. The clock frequency f_{CLK} was 20 MHz and the frequency control word K was 48, hence, the fundamental frequency of the synthesizer output f_{TFF} was expected to be 3.75 MHz. Division ratio of the frequency divider N was selected to be 8. Fig. 14 shows that V_{TFF} was a square waveform with duty cycle of exactly 50%.

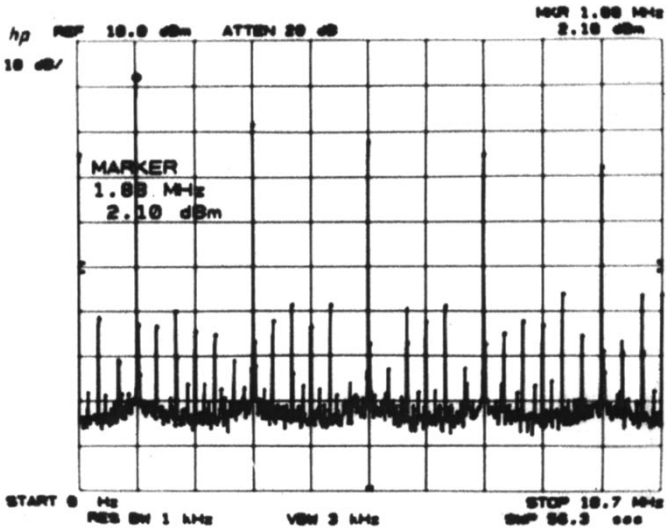


Fig. 12. Spectrum of the frequency synthesizer with static D/A's. H: DC-18.7 MHz, V: 10 dB/div.

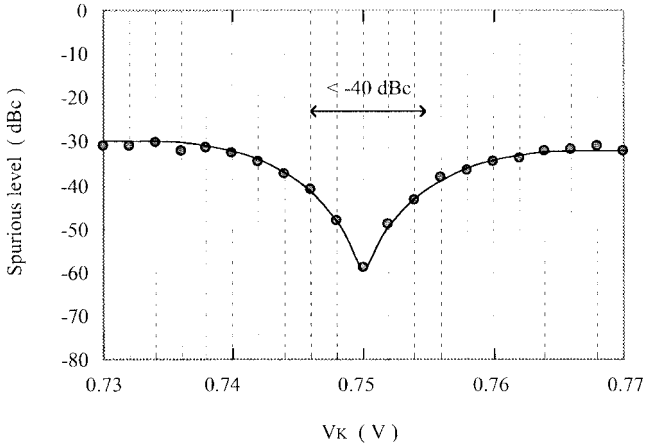
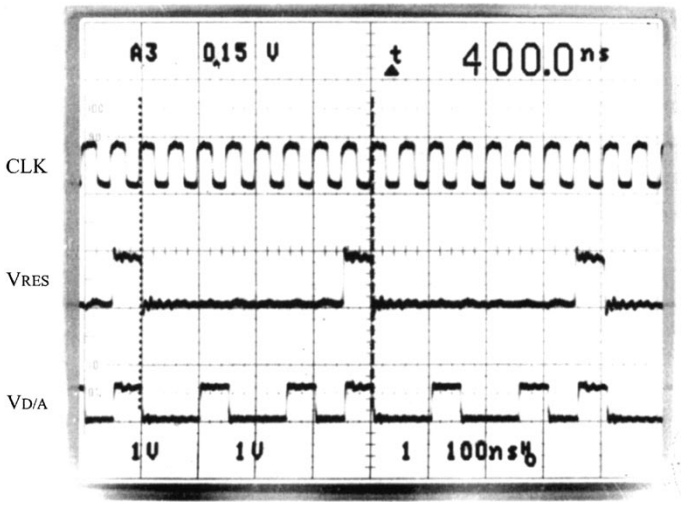
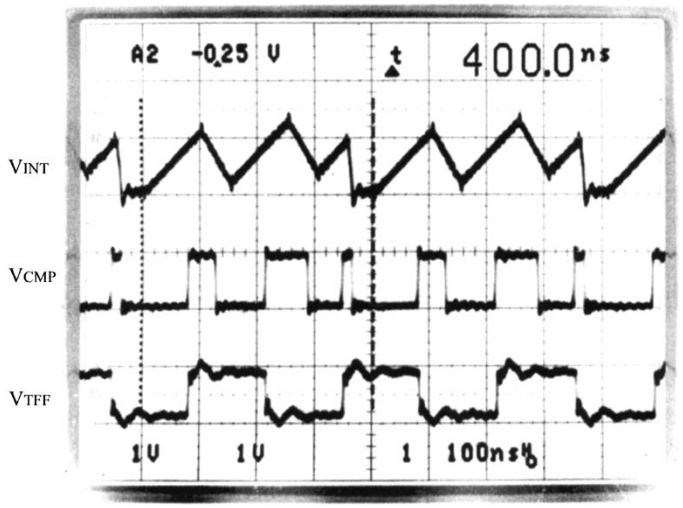


Fig. 13. Relation between V_K and spurious level.



(a)



(b)

Fig. 14. Measured waveforms of the frequency synthesizer with a dynamic D/A.

Fig. 15 shows the spectrum of V_{TFF} for the frequency control word $K = 48$ and a higher clock frequency $f_{\mathrm{CLK}} = 50$ MHz. In this figure, the spectrum of V_{TFF} includes the

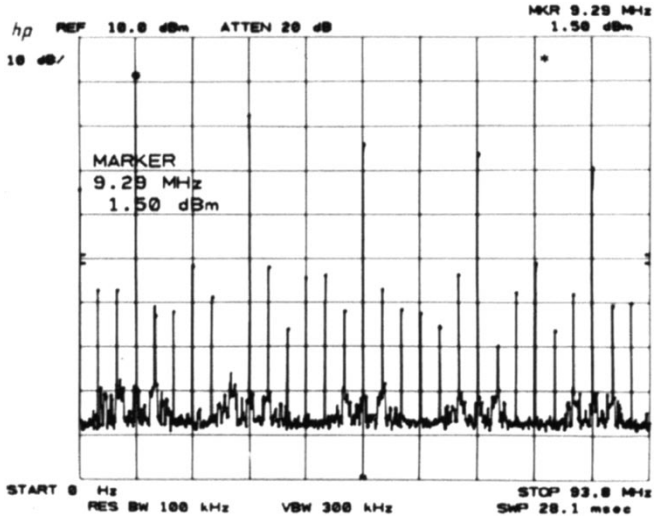


Fig. 15. Spectrum of the frequency synthesizer with a dynamic D/A. H: DC-93.8 MHz, V: 10 dB/div.

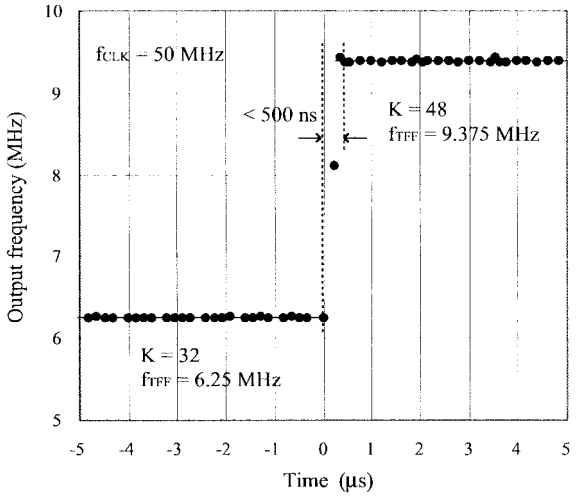


Fig. 16. Time dependence of the output frequency during frequency switching.

fundamental frequency 9.375 MHz and its harmonics, and the highest spurious level, excluding the harmonics, is −45 dBc.

Fig. 16 shows the time dependence of the output frequency during frequency switching, as measured by a frequency and time-interval analyzer (HP5372A). The frequency control word $K = 32$ corresponded to the output fundamental frequency 6.25 MHz, and $K = 48$ corresponded to 9.375 MHz. This result shows that the frequency switching is completed within less than 500 ns.

We are now integrating an 8-b DAC (with $V_{FS/2}$ output) with a high-speed Si bipolar process [9]. This DAC can operate at a 1-GHz clock input. The proposed frequency synthesizer is expected to be used for local oscillators in microwave communication equipment. For high-frequency applications, an up-converting technique can be applied using a constant-frequency microwave-signal generator.

IV. Conclusion

A new direct frequency synthesizer whose power consumption is significantly lower than the ROM-less DDS's

has been developed. We proposed two types of integrators for the frequency synthesizer: a very low-power integrator that uses static D/A's and an integrator that uses a dynamic D/A and has a high-speed capability. Experimental results showed that the frequency synthesizer creates square waves with low spurious components. The digital resetting circuit, which consists of the frequency divider and the PWAC, was effective in restraining frequency drift in the output signal. The proposed architecture can be applied to high-speed and low-power frequency synthesizers for wireless communication systems that require fast frequency switching.

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Hideyuki Nosaka (M'97) was born in Kanagawa, Japan, on March 4, 1971. He received the B.S. and M.S. degrees in physics from Keio University, Kanagawa, Japan, in 1993 and 1995, respectively.

In 1995, he joined NTT Wireless Systems Laboratories, Yokosuka, Japan, where he is engaged in the research and development of monolithic microwave integrated circuits (MMIC's) and microwave synthesizers.

Mr. Nosaka is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan.

Tadao Nakagawa (M'91) was born in Kobe, Japan, on July 21, 1963. He received the B.E. and M.E. degrees in material physics and the Dr. Eng. degree in communication engineering from Osaka University, Osaka, Japan, in 1986, 1988, and 1997, respectively.

In 1988, he joined NTT Radio Communication Systems Laboratories, Yokosuka, Japan, where he was engaged in the research and development of MMIC's and microwave synthesizers. Since 1997, he has been an Associate Manager at STE Telecommunication Engineering Company, Ltd., Tokyo, Japan, where he is a Technical Consultant on wireless communications to Seiko Epson Corporation, Nagano, Japan.

Dr. Nakagawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He received the Young Engineer Award from the IEICE in 1995.

Akihiro Yamagishi was born in Toyama, Japan, in 1964. He received the B.E. and M.E. degrees from Toyama University, Toyama, Japan, in 1986 and 1988, respectively.

In 1988, he joined NTT LSI Laboratories. He is currently with NTT System Electronics Laboratories, Kanagawa, Japan. His research interests include the research and design of synthesizer large-scale integrations (LSI's).